Design methodology in multiphase buck converter based on minimum time control for high efficiency RF amplifiers

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***Abstract*—This paper proposes an interleaved multiphase buck converter with minimum time control strategy for envelope amplifiers in high efficiency RF power amplifiers. The solution of the envelope amplifier is to combine the proposed converter with a linear regulator in series. High system efficiency can be obtained through modulating the supply voltage of the envelope amplifier with the fast output voltage variation of the converter working with several particular duty cycles that achieve total ripple cancellation. The transient model for minimum time control is explained, and the calculation of transient times that are pre-calculated and inserted into a look-up table is presented. The filter design trade-off that limits capability of envelope modulation is also discussed. The experimental results verify the fast voltage transient obtained with a 4-phase buck prototype.**

I. Introduction

THE communication systems use non-constant envelope RF signals associated with spectrum-efficient digital modulations in order to increase the channel capacity. Unfortunately, the linear power amplifiers (such as class A, B or AB) have low efficiency with non-constant envelope signals, especially, when signals with high peak to average power ratio envelope are transmitted. Envelope elimination and restoration (EER) technique can improve efficiency of RF power amplifier systems by using a highly efficient switched-mode power supply to track signal envelope. Fig. 1 shows the block diagram of EER technique. The main challenge to realize high efficiency EER system is to implement high efficiency envelope-tracking power converter. Several solutions have been proposed in the state of the art. A very efficient switching converter with digital control is described in [1], but the efficiency drops down significantly when the bandwidth of envelope increases. The interleaved multiphase converter in [2] also has this limitation. In [3], the three-level buck converter is good for low-power portable device application. These solutions with only switch-mode converter have significant power losses in wide-bandwidth envelope application, because the switch frequency has to be much higher that envelope bandwidth, which leads to high switching power losses. To achieve large bandwidth tracking without pushing switch converter working at extremely high frequency, switch-mode converter combined with linear regulator is a suitable solution. In [4], a linear assisted DC/DC converter is a parallel combination of a multiple input buck converter and linear regulator. Another idea is a multilevel switched converter in series with a high slew rate linear regulator [5].

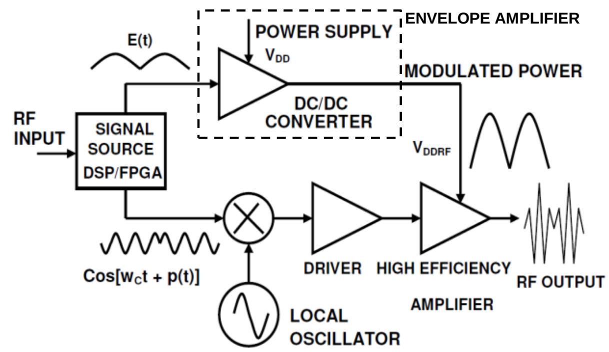

Fig. 1 Simplified block diagram of EER technique

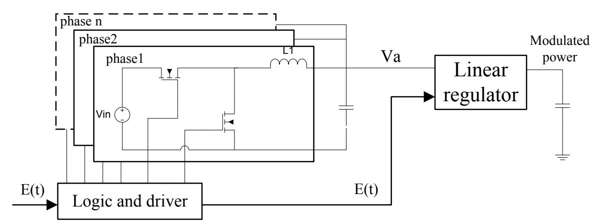

Fig. 2 Simplified schematic of proposed envelope

This paper is based on the solution [5], but replacing the multilevel converter by a multiphase DC-DC converter, in Fig. 2. The multilevel converter can provide discrete output voltage through several independent voltage cells in series. And the proposed solution implements the minimum time control to achieve fast transitions between some pre-defined voltage levels, shown in Fig. 3. Comparing these two solutions, the

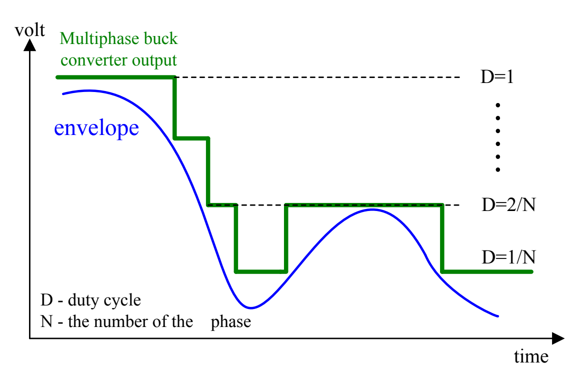

Fig. 3 Time diagrams of the envelope amplifier

proposed one has smaller size, higher efficiency, but more complex control.

II. Minimum Time Control Strategy

The principle of Minimum time control is explained in [6-7]. If the buck converter is considered as a linear system, there are two parameters can be used to describe the state of converter, the inductor current and output voltage. The method of minimum time control is to change the buck converter from the initial state to the target state through on-off switching actions and the simplest way is to have a single on-off switching action [8], which is discussed here. The challenge is to get the function of minimum time based on an accurate converter model.

Most of work on the minimum time control that have been proposed overlook the ripples, but when the minimum time is so small (such as one switching cycle), the ripples cannot be neglected. Due to this reason, this paper proposes the minimum time control strategy based on charge balance method and take the inductor current ripple into account. In order to apply the control strategy properly, the interleaved converter works at the duty cycles (i/n, i=1, 2 … n, n is the number of phase, like in Fig. 3) that lead to completely voltage cancellation. And it is assumed that output voltage changes linearly during transient time that is close to actual response. Therefore the output voltage during the transition will be:

$$V_{out}(t) = V_1 + \frac{\Delta V}{\Delta t}\cdot t \tag{1}$$

V_1 is initial output voltage, Δt is the transition time and ΔV is the difference of target output voltage and initial output voltage. Both the charge on the capacitor and the charge to the load come from all the phases and it can be expressed as:

$$\sum\nolimits_{\mathrm{i=1}}^{\mathrm{N}} \mathrm{Q_{Li}} = \mathrm{Q_C} + \mathrm{Q_{LOAD}} = C\cdot\Delta V + \mathrm{Q_{LOAD}} \tag{2}$$

where Q_{Li} is the charge provided by each phase of the multiphase converter. For step-up transition, the main switch will be first on and then off. The output capacitor will be charged. With linearly output voltage change, it can be written (assume that each phase has the same Δt):

$$Q_{Li} = -\frac{V_{in}}{2L}t_{ON,i}^2 - \frac{V_1}{2L}\Delta t^2 + \frac{V_{in}t_{ON,i}\Delta t}{L} + I_i\Delta t - \frac{\Delta V\Delta t^2}{6L} \tag{3}$$

For step-down transition, the main switch will be first off and then on. The output capacitor will be discharged. The charge from each phase is expressed as:

$$Q_{Li} = \frac{V_{in}}{2L}t_{ON,i}^2 - \frac{V_1}{2L}\Delta t^2 + I_i\Delta t - \frac{\Delta V\Delta t^2}{6L} \tag{4}$$

where I_i is the i^{th} inductor's current before the transient, $t_{ON,i}$ is the time interval during which the main switch of the i^{th} phase is turned on and L is the value of the inductor in each phase. For both step-up and step-down transition, the relationship between Δt and $t_{ON,i}$ can be found as:

$$t_{ON,i} = K\Delta t + \frac{L\Delta I_i}{V_{in}},\quad K = \frac{V_1 + \Delta V/2}{V_{in}} \tag{5}$$

where ΔI_i is the difference of the i^{th} phase inductor current between the initial and the target state.

As mentioned earlier, the converter's steady state is at the duty cycles with complete ripple cancellation. Therefore, the following equation always holds that,

$$\sum\nolimits_{i=1}^{N}\Delta I_i = 0 \tag{6}$$

With (5) and (6) it can be obtained,

$$\sum\nolimits_{i=1}^{n} t_{on,i} = nK\Delta t \tag{7}$$

$$\sum\nolimits_{i=1}^{n} t_{on,i}^2 = nK^2\Delta t^2 + \frac{L^2}{V_{in}^2}\sum\nolimits_{i=1}^{n}\Delta I_i^2 \tag{8}$$

The equation to calculate Δt for step-up transition can be obtained by using (2), (3), (7) and (8) (in this application, it is assumed that the output voltage changes sufficiently fast so that the load current can be seen as constant during the transition time).

$$C\Delta V = \Delta t^2\left(-\frac{V_{in}}{2L}nK^2 + \frac{V_{in}}{L}nK - \frac{V_1}{2L}n - \frac{\Delta V}{6L}n\right) - \frac{L}{2V_{in}}\sum\nolimits_{\mathrm{i=1}}^{\mathrm{N}}\Delta I_i^2 \tag{9}$$

And also the equation to calculate Δt for step-down transition can be obtained by using (2), (4), (7) and (8).

$$C\Delta V = \Delta t^2\left(\frac{V_{in}}{2L}nK^2 - \frac{V_1}{2L}n - \frac{\Delta V}{6L}n\right) + \frac{L}{2V_{in}}\sum\nolimits_{\mathrm{i=1}}^{\mathrm{N}}\Delta I_i^2 \tag{10}$$

From (9) and (10) it can be seen that all the parameters that are necessary to calculate Δt and $t_{ON,i}$ can be obtained except $\sum_{i=1}^{N}\Delta I_i^2$. However, if the transient is synchronized with PWM duty cycle, ΔI_i can be calculated through input voltage, duty cycle, inductance and phase shifting. One of the synchronizing ways is to start the transient at the end of PWM cycle of one phase (rising or falling edge). At this moment, all the phases enter the minimum time control and each phase will have different on-time and off-time, but the same transition time. Then the minimum time control will end at the beginning of PWM cycle of that phase (rising or falling edge) and keep the

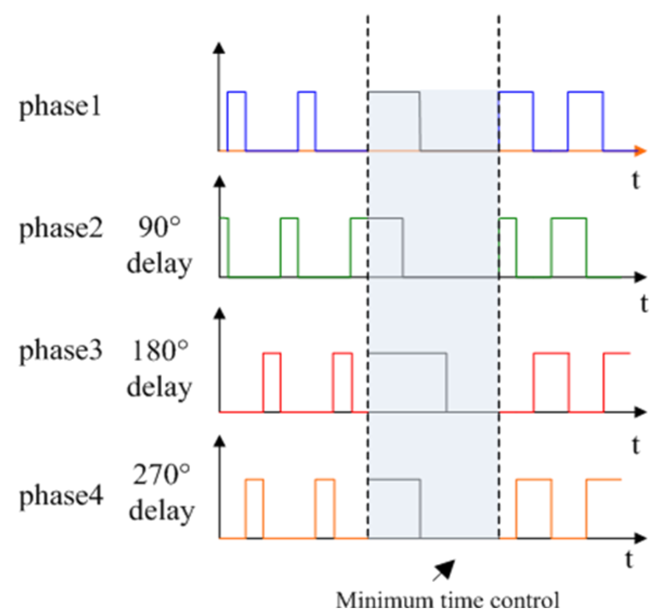

Fig. 4 Control strategy for the voltage transition from $0.25V_{IN}$ to $0.5V_{IN}$

corresponding phase delay for the rest phases, which is used in this paper, shown in Fig. 4. In this way, ΔI_i for each phase can be exactly calculated. Additionally, the factor that affects the transient time will be the sum of the inductor current difference of each phase, not the current of each phase itself, which indicates that a good inductor currents balance is not necessary in this model. And the converter switching frequency f_{SW} is a parameter to obtain ΔI_i, therefore it also has influence on Δt and $t_{ON,i}$.

III. Filter Design Constraint

The inductor limits the slew rate of current through the output capacitor, and the output capacitance value determines the charge that has to be delivered during the transient time to change the output voltage. Therefore the output filer (L, C) limits the response time of the buck converter to change the output voltage. And this transient time restrict the maximum bandwidth of the envelope that the converter can modulate. The transient time that the converter needs to change from one state to another one can be calculated through filter parameters. However, the design way is usually inversed. The maximum transient time of the converter that can be accepted is fixed by application (such as the specifications of the transmitted signal). For the given maximum signal slope, there are a plenty of possibilities for the filter parameters (L, C). Fig. 5 shows the constraint of the filter to track the maximum envelope slope of 52.4 volts/us. The combinations of L, C and f_{SW} on the surface are the minimum requirement in order to track that envelope. Additionally, to design for very fast output voltage transient, a high ratio between L and C is suitable for charging output capacitor very fast. And it makes inductor size large. On the other hand, the good regulation under the load current change requires a low ratio between L and C. It reduces the size of inductor, but increases the inductor current ripple and output voltage ripple. Therefore, the transient speed and regulation tradeoff is necessary for a specific design.

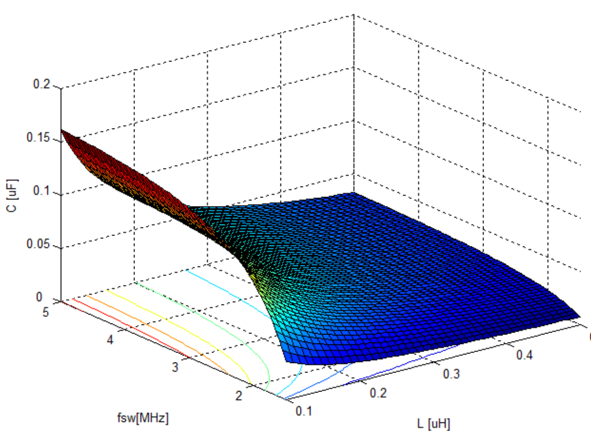

Fig. 5 a constraint of the filter design from output 3V to 9V

IV. Experimental Results

The design and control methodology are validated with a four phases buck prototype. The converter parameters are, V_{IN} = 12V, L = 6.8uH, C = 1uF. Fig. 6 and Fig. 7 show the output change from 3V to 6V (25% duty cycle to 50%) and from 9V to 6V (75% duty cycle to 50%). In this envelope amplifiers application, the load of the buck converter is a linear regulator, which behaves as a current source. If the output voltage changes much faster than reference changes, the load current can be considered constant during the transient time. Additionally, the sum of the phase currents will not change after the transient, which indicates that the control algorithm is not influenced by the load current. Fig. 8 shows the performance of the implemented interleaved multiphase buck converter in envelope tracking. The envelope reference is a 20kHz sinusoidal waveform and the discrete output voltage level can be 3V, 6V, 9V and 12V. The measured envelope amplifier efficiency is up to 80%. Fig. 9 shows the envelope amplifier performance with 50kHz reference. It can be seen that there are only two output voltage level in order to track the envelope, because it is not fast enough to apply all the levels. This shows the flexibility of the control strategy which

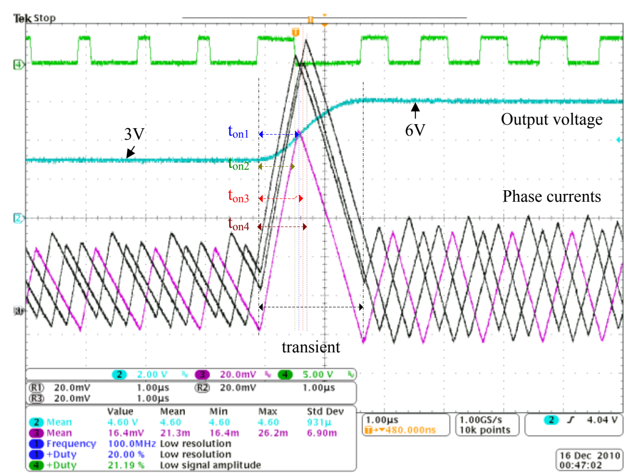

Fig. 6 Output voltage step from 3V to 6V, 1MHz (2V/div) and Phase currents (200mA/div)

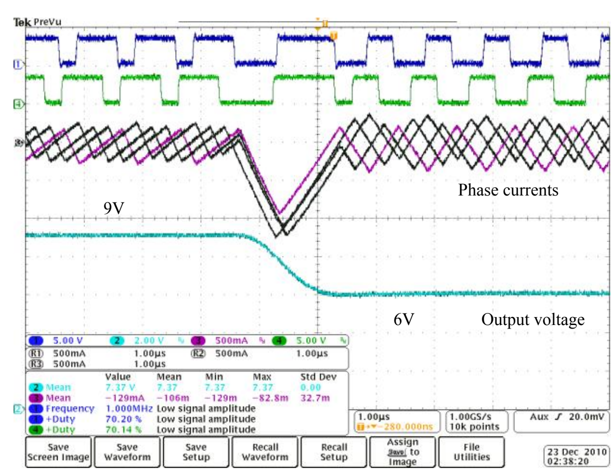

Fig. 7 Output voltage step from 9V to 6V, 1MHz (2V/div) and Phase currents (500mA/div)

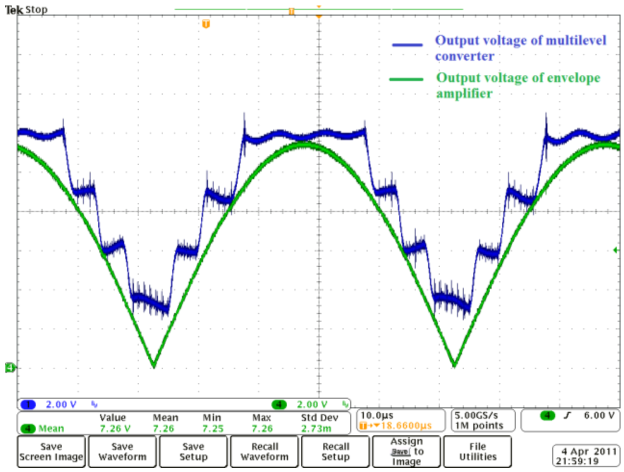

Fig. 8 Output voltage of multilevel converter and envelope amplifier with 20kHz reference (2V/div)

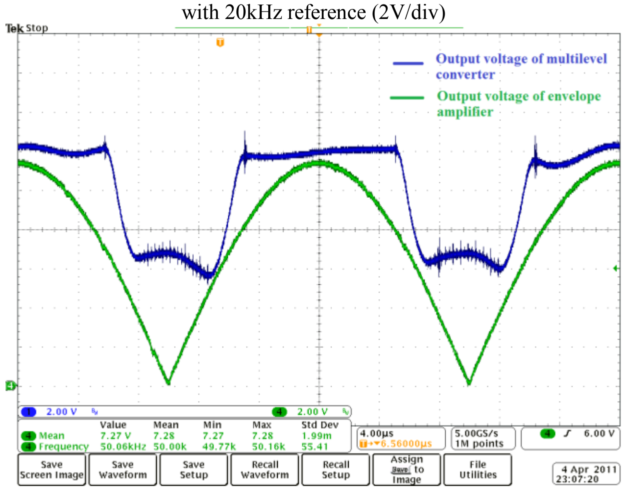

Fig. 9 Output voltage of multilevel converter and envelope amplifier with 50kHz reference (2V/div)

is also an advantage in this application, because it helps the converter to track high slew rate change envelope with relatively low switching frequency. And the system efficiency (envelope amplifier) measured is 76.5%. Both measurements use 10 ohms resistor as load.

V. CONCLUSIONS

The new solution of implementation of highly efficient envelope amplifier in EER technique is explained in this paper. An interleaved multiphase buck converter with minimum time control strategy in series with a linear regulator can be a high efficiency solution for EER technique envelope amplifiers. The model of minimum time control is presented and filter design is discussed in order to meet the requirement for the variations of output voltage. And it is important to notice that there is no current measure requirement for the minimum time control, which makes the implementation very simple. The performance of the converter of the envelope amplifier that is obtained with a 4-phase buck prototype confirms that the steady state is re-established after transient time, which is anticipated in theory. The integration of the RF power amplifier with proposed envelope amplifier and measure of the system efficiency will be the future work.

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